Self-Aligned InGaAs FinFETs with 5-nm Fin-Width and 5-nm Gate-Contact Separation

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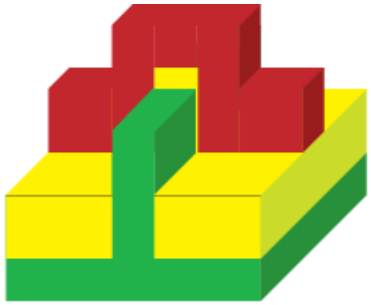
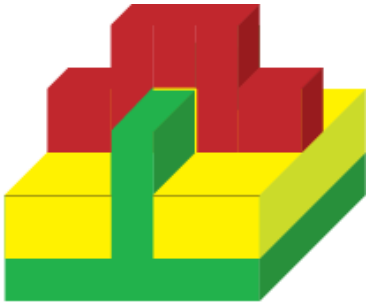
FinFETs

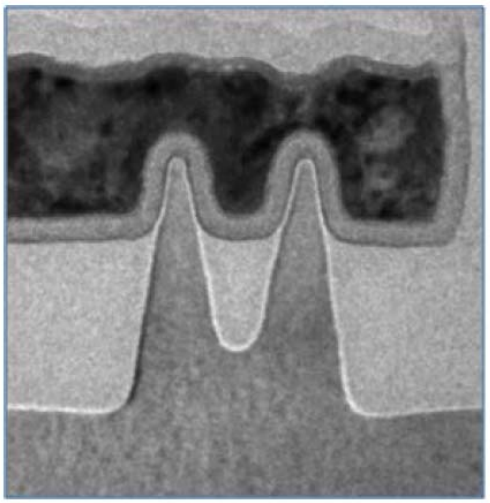
Double gate



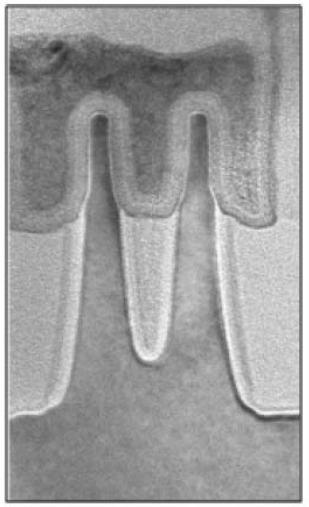
Tri gate



Intel Si Trigate MOSFETs



22 nm Process



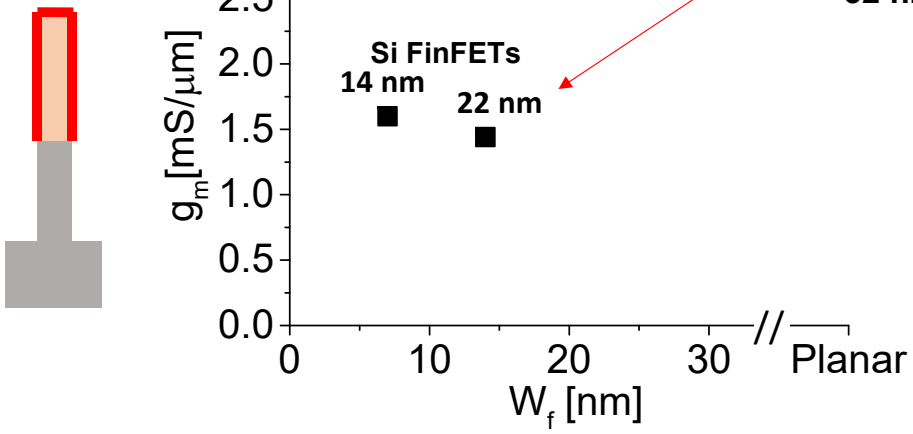
14 nm Process

FinFETs used in state-of-the-art Si CMOS

- improved short-channel effects
- smaller footprint
- but… higher parasitics

Si and InGaAs FinFETs

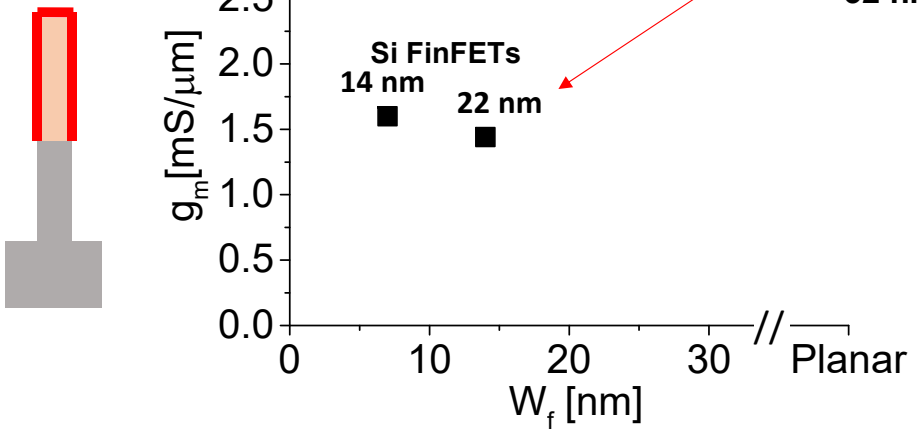
normalized by gate periphery



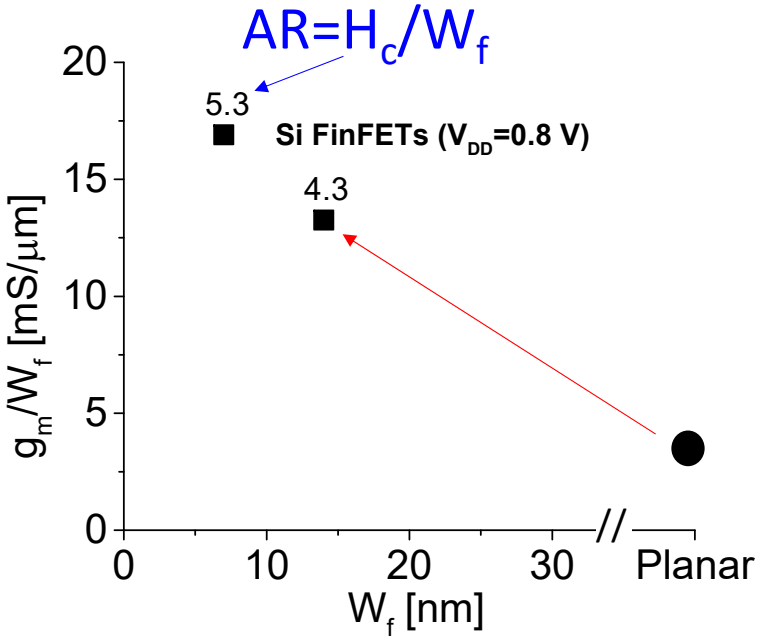
- Si planar → FinFET: performance ↓

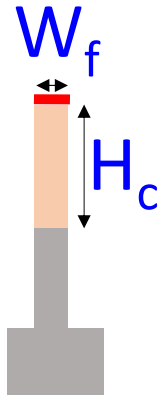
Si and InGaAs FinFETs

normalized by gate periphery



normalized by fin footprint

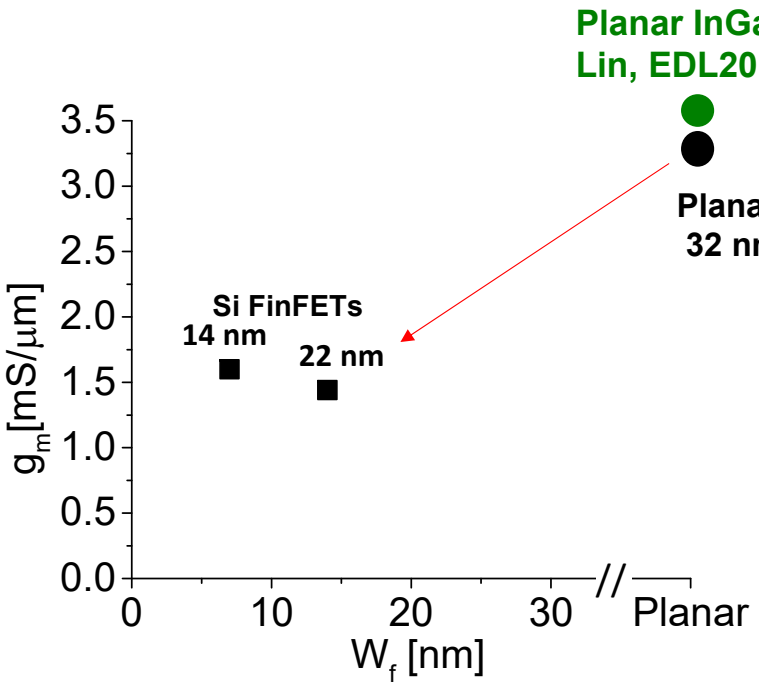




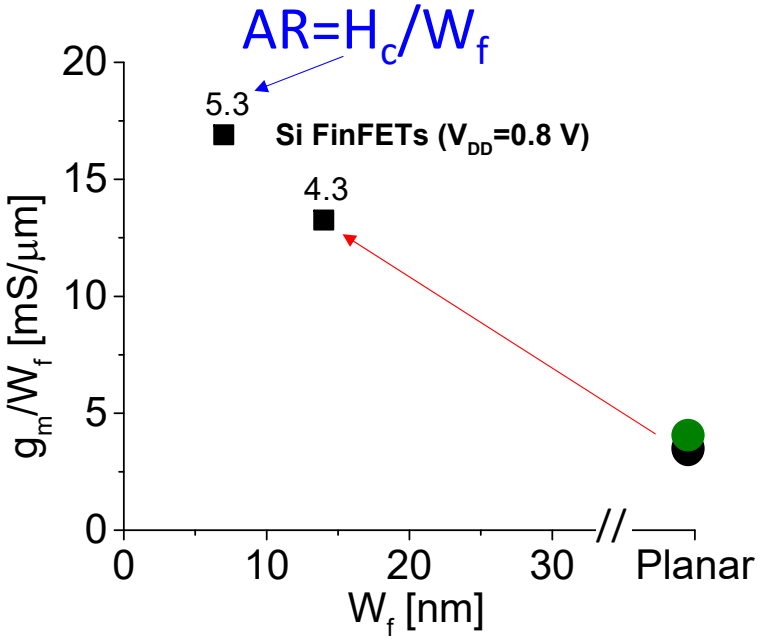
- Si planar → FinFET: performance ↓, performance per footprint ↑
- Key challenge for FinFETs → efficient transport on sidewalls

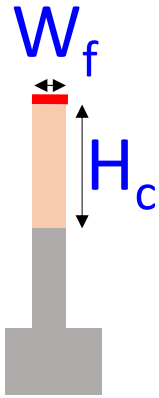
Si and InGaAs FinFETs

normalized by gate periphery



normalized by fin footprint

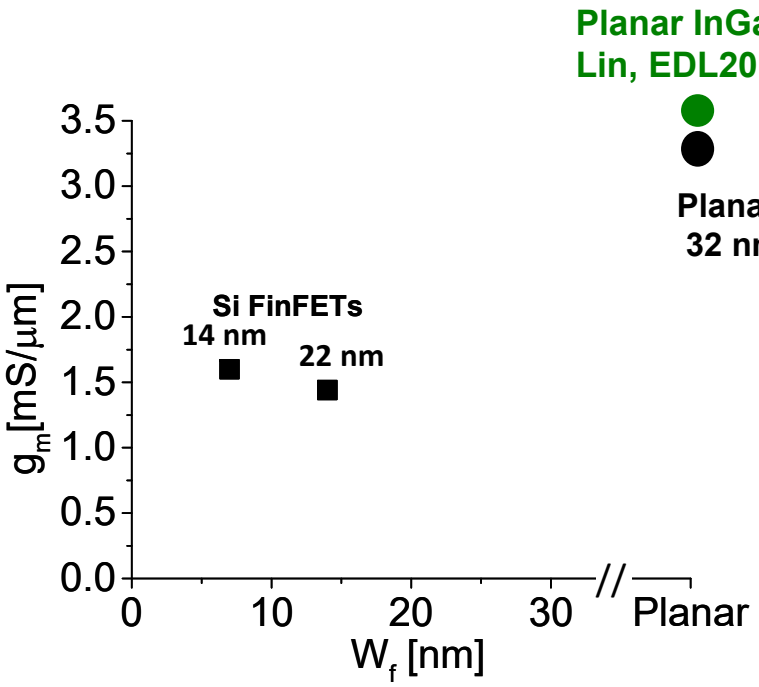




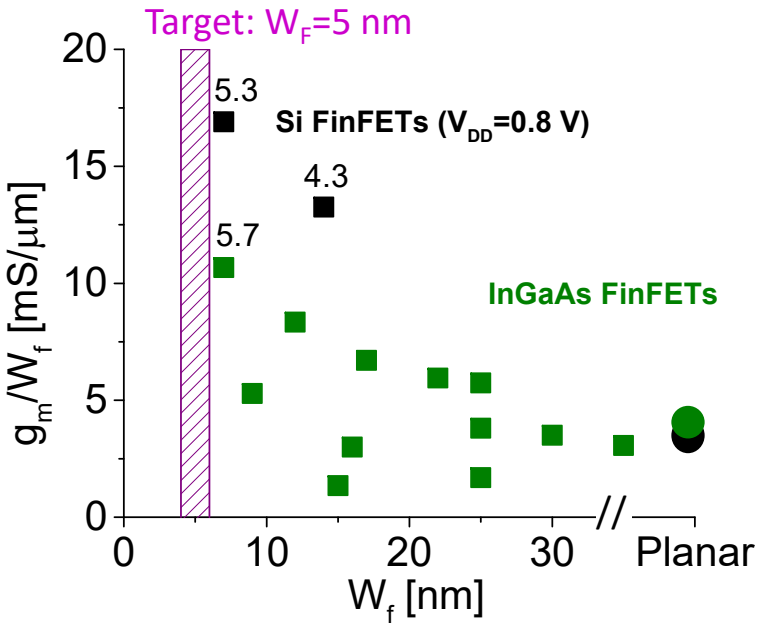
- III-V planar ~ Si planar

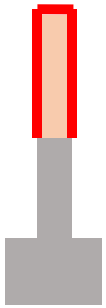
Si and InGaAs FinFETs

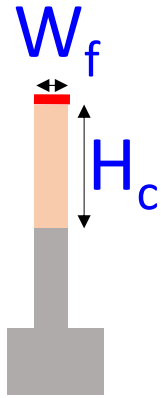
normalized by gate periphery



normalized by fin footprint



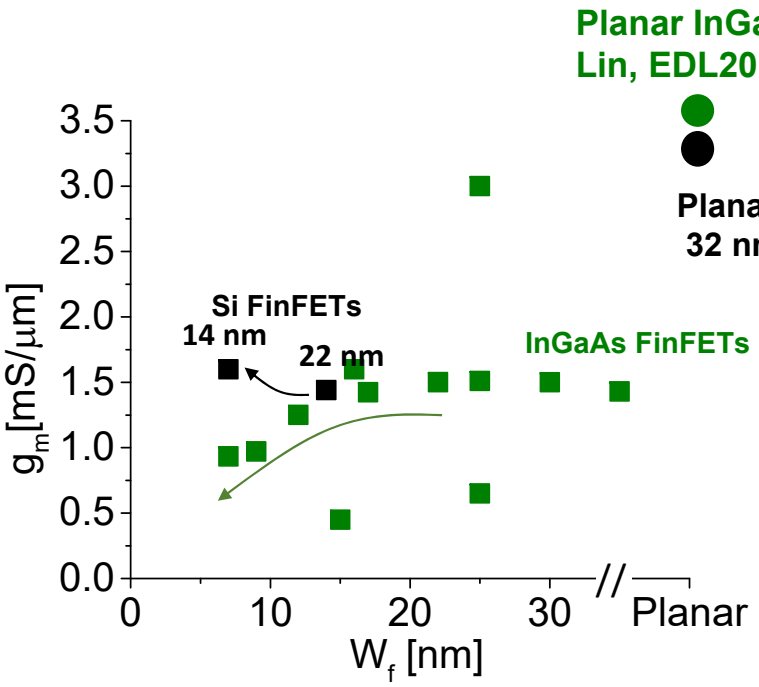




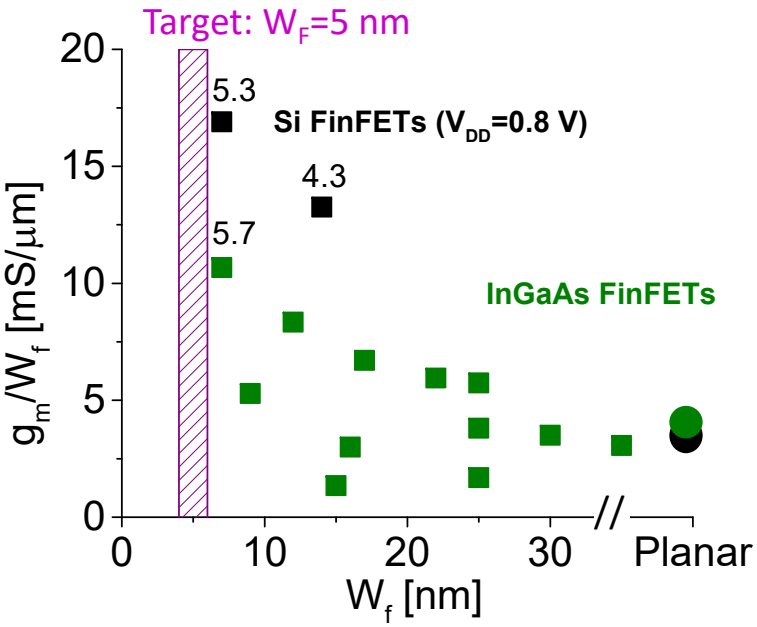
- g_m(III-V FinFETs) < g_m(Si)
- Target of W_f=5 nm yet to be demonstrated

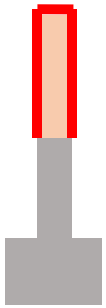
Si and InGaAs FinFETs

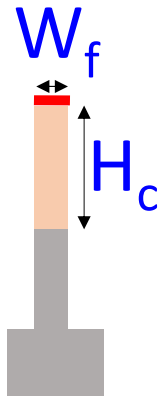
normalized by gate periphery



normalized by fin footprint

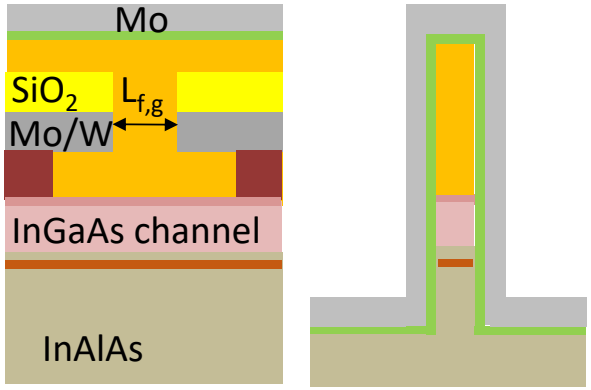


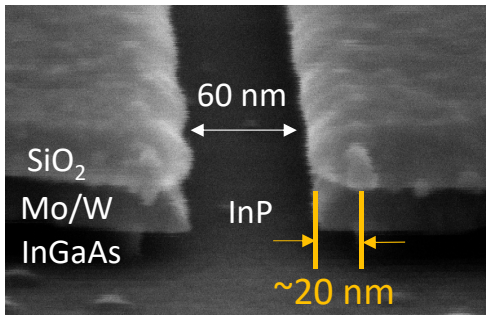




- III-V FinFET: W_f< 20 nm → g_m ↓
- Challenge: Improve III-V sidewall conductivity

MIT InGaAs FinFET's Gen. #2 vs. #1



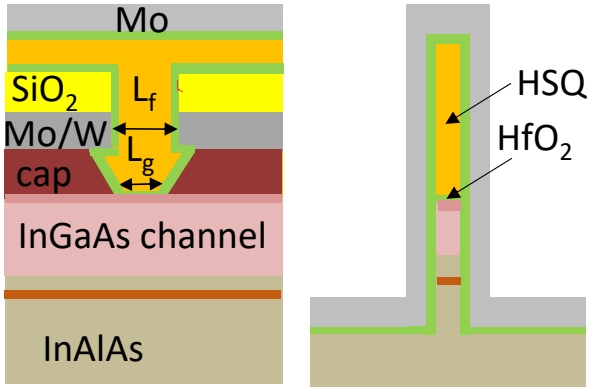


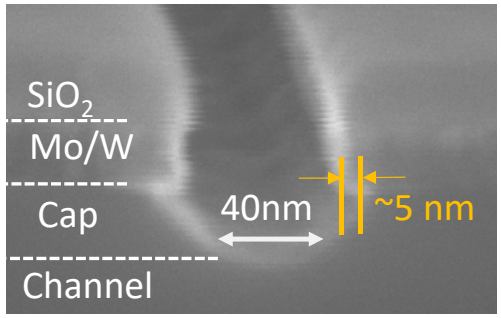
Wet recess

Gen. #1: Vardi et al., VLSI 2016, EDL 2016

Gen #1:

- Wet cap recess
- 3 Digital etch cycles
- 40 nm channel height
- δ-doping





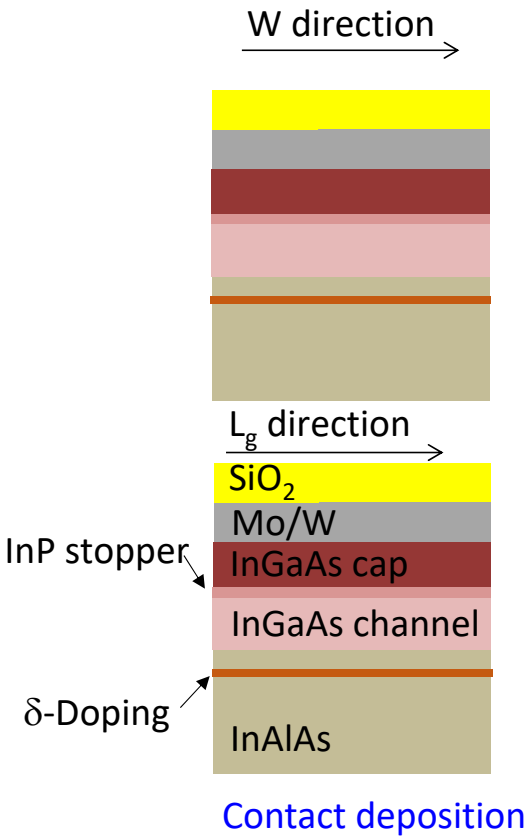
Dry+DE recess

Gen. #2: This work

Gen #2:

- Dry cap recess
- 5 Digital etch cycles
- 50 nm channel
- Fin-top passivation
- Remove δ-doping (in 2nd stage)

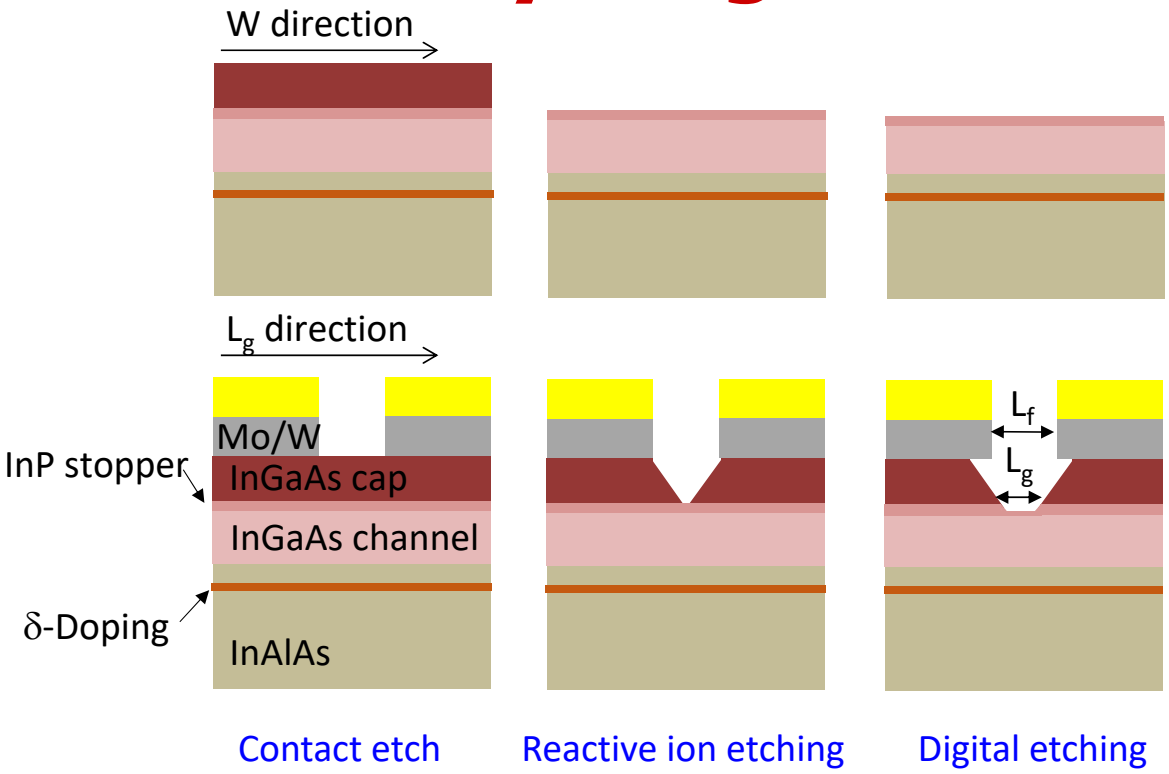
Process Technology: contact-first

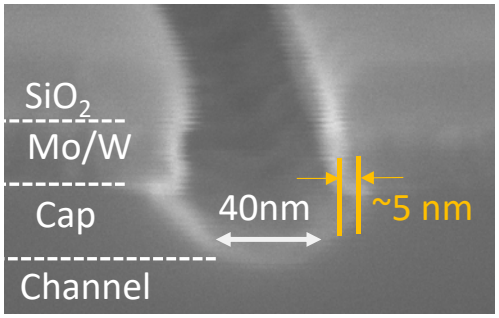


Lin, IEDM 2013
Lu, EDL 2014
Vardi, EDL 2014

- Yield $R_C < 10\ \Omega{\cdot}\mu m$

Dry+Digital Etch cap recess



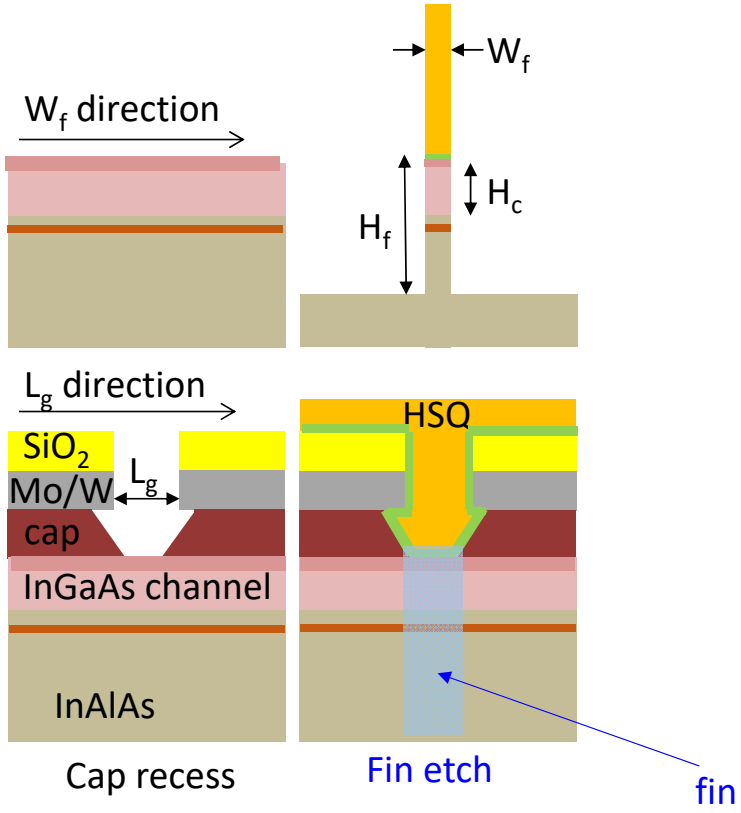


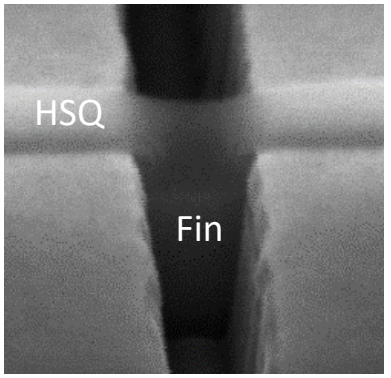
Dry+DE recess

- No metal pullback
- III-V cap pullback only during digital etch

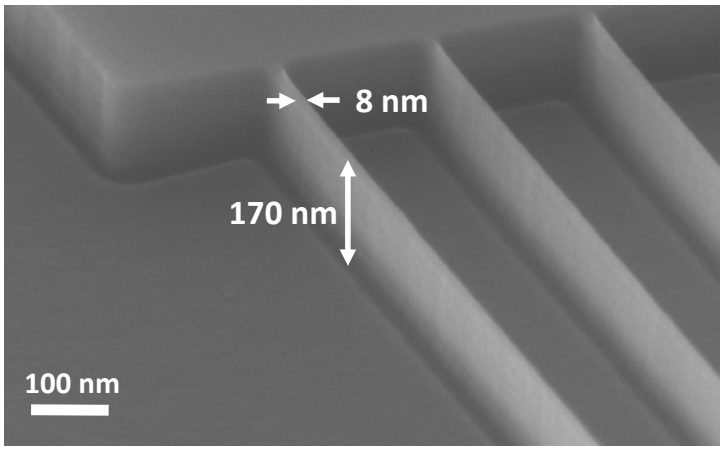
(Lin, IEDM 2013)

Dry+Digital Etch fin definition



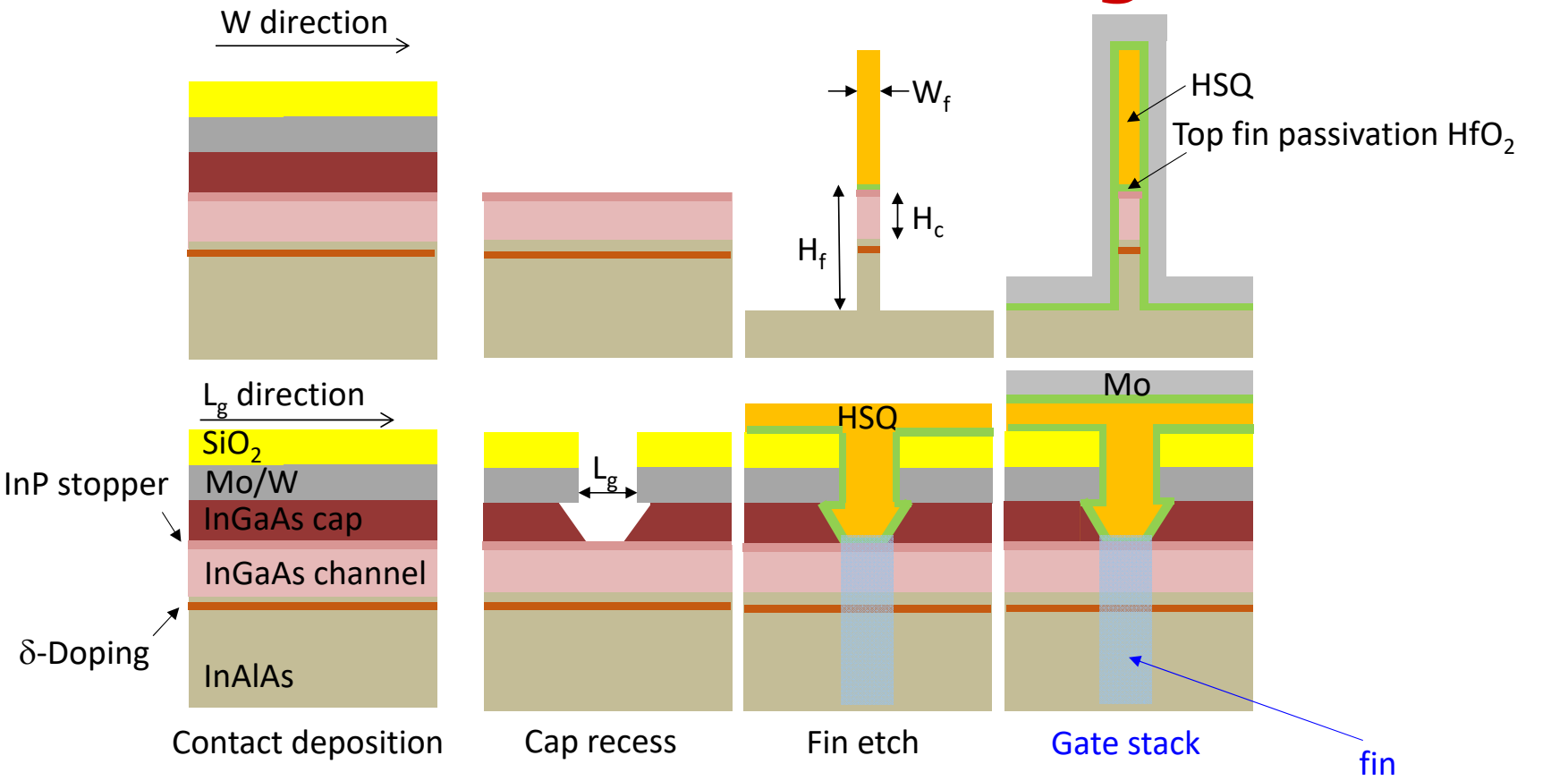


Zhao, EDL 2014, Vardi, VLSI 2016



- $BCl_3/SiCl_4/Ar$ RIE + 5 DE cycles : smooth, vertical sidewalls and high aspect ratio (>10)

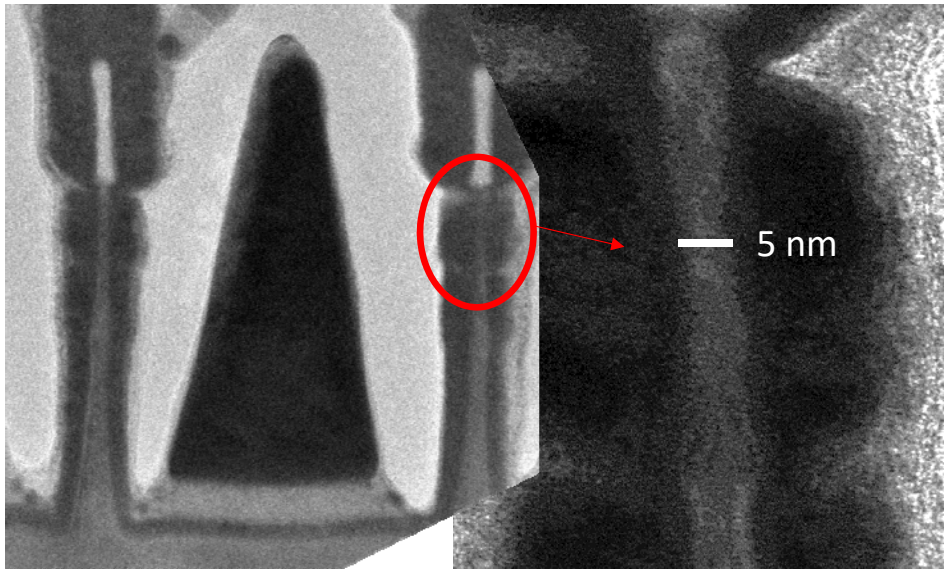
Gate stack - Double gate FinFET



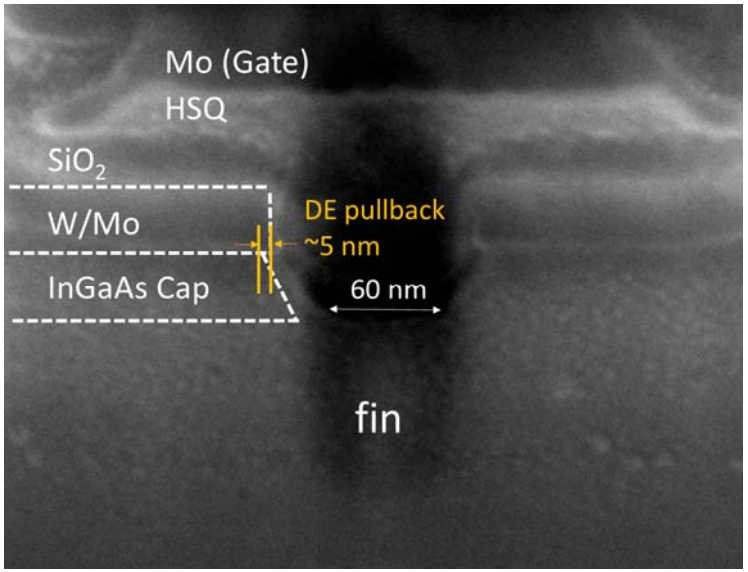
- HSQ stays on top of fins
  → double-gate FinFET
- Gate oxide – 3 nm HfO_2 (vs. 2.3 nm in EDL2016)

Device cross section

TEM of finished device in W_f direction

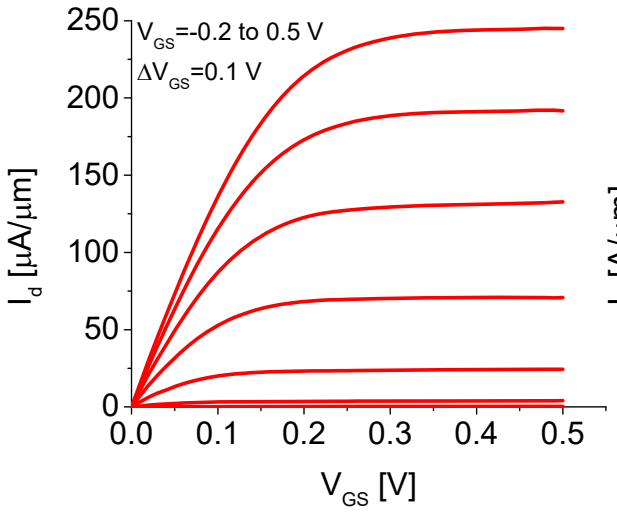


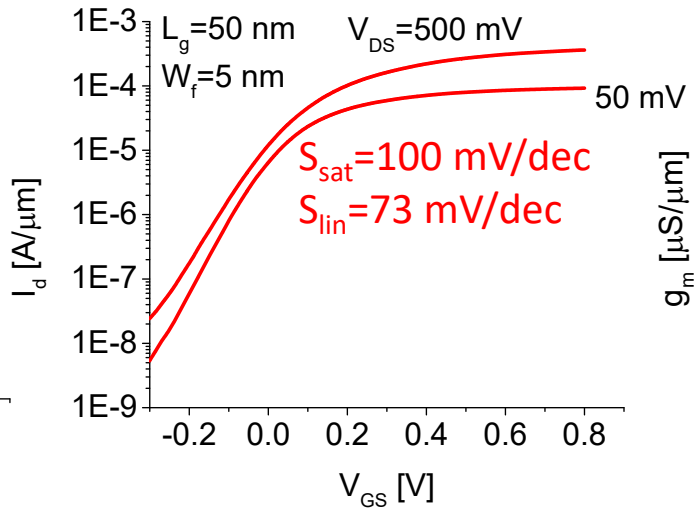
FIB cross section in L_g direction

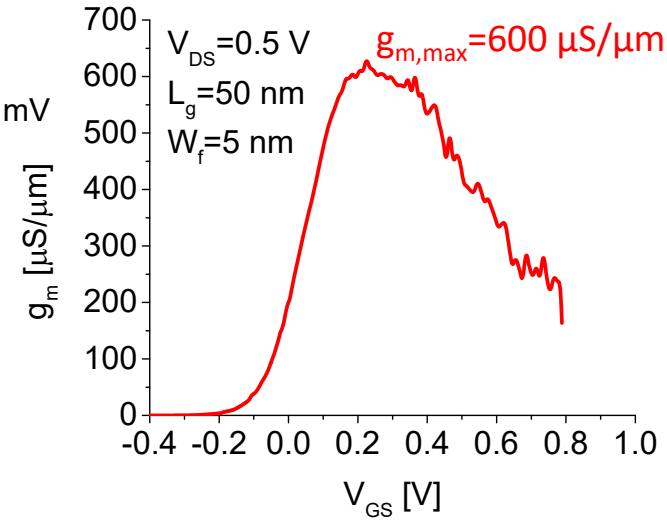


- Fin pitch: 200 nm
- 10-200 fins/device
- W_f : 5-25 nm
- L_g : 30 nm – 5 µm
- Contact to channel separation set by DE : ~5 nm

Electrical characteristics: W_f=5 nm, L_g=50 nm



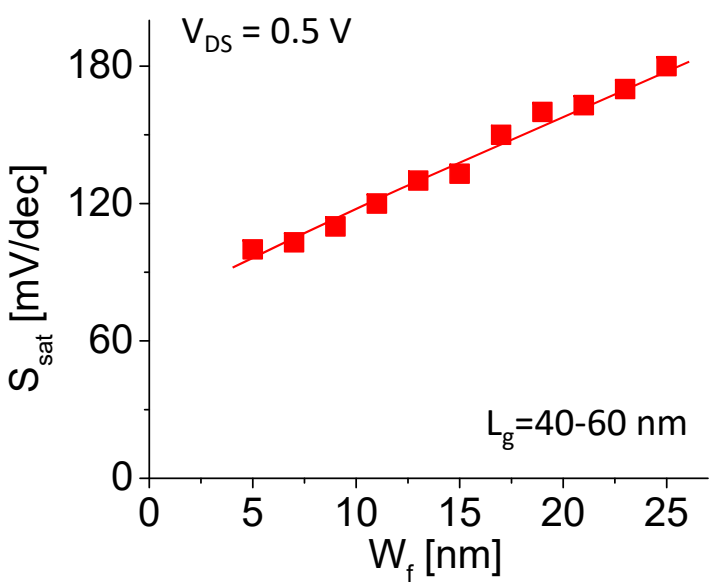


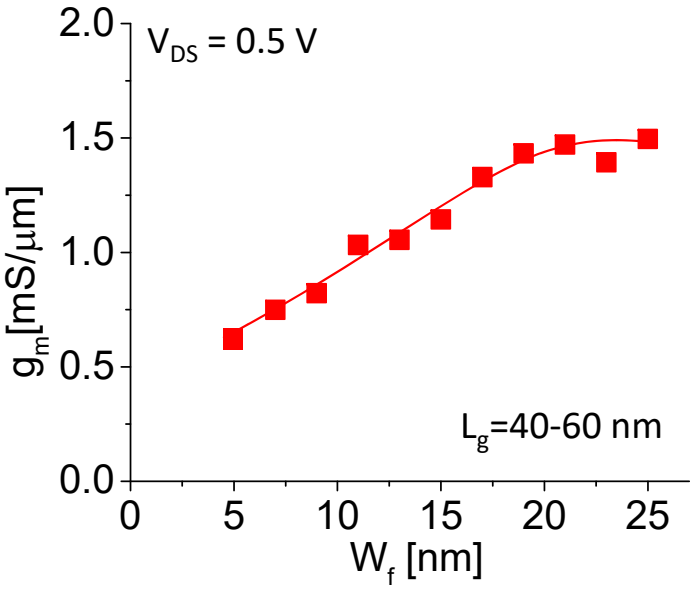


Normalized by gate periphery

- Well behaved devices with W_f=5 nm

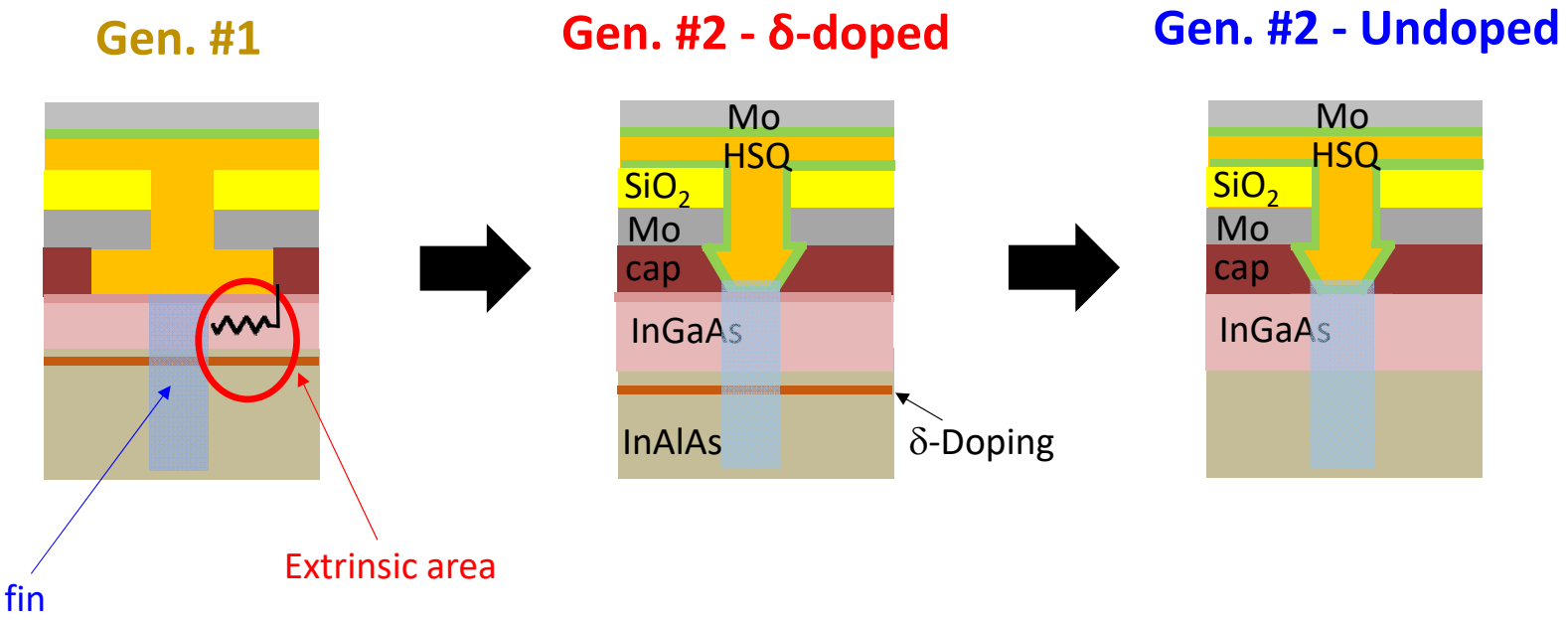
On/Off performance: fin width scaling





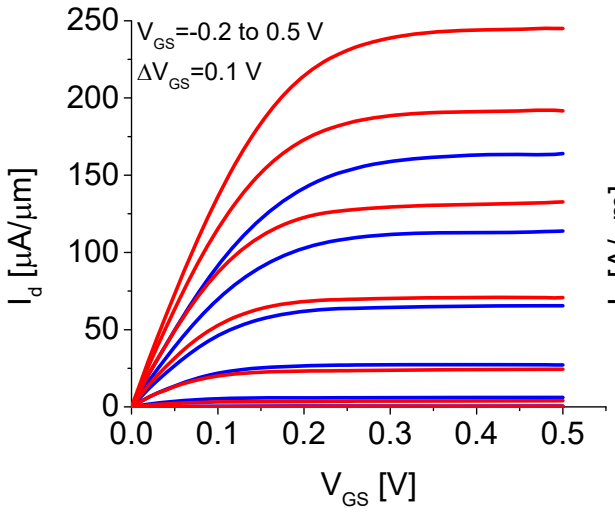
- $W_f \downarrow$: $S_{sat} \downarrow$
- $W_f \downarrow$: $g_m \downarrow$

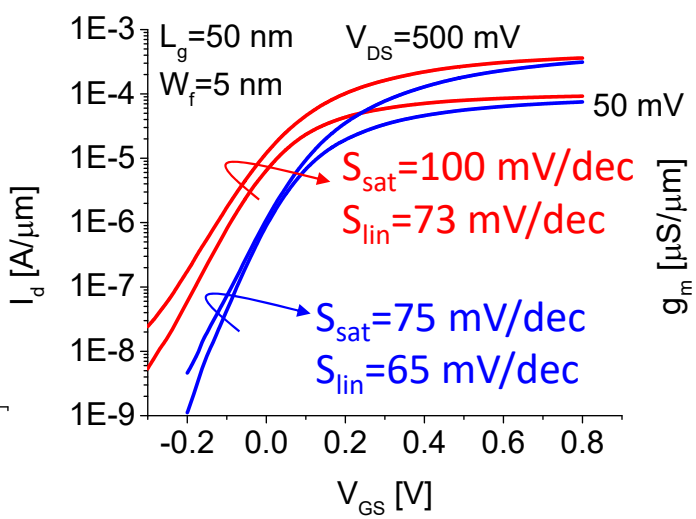
To improve Off performance: remove δ-doping

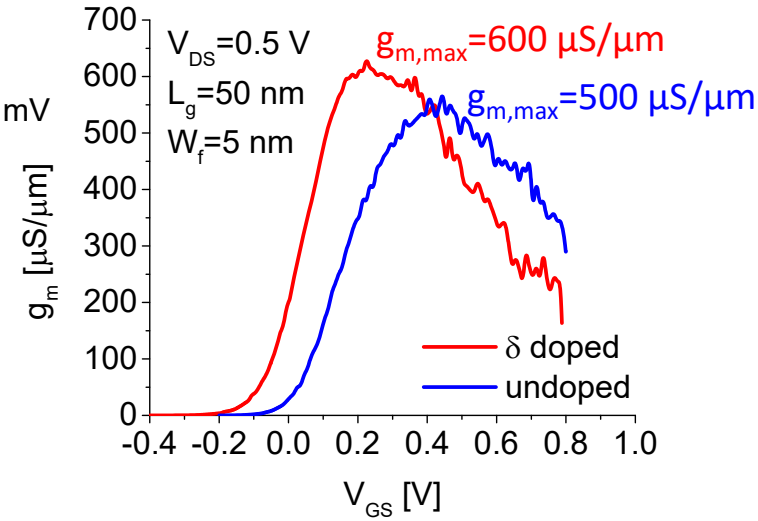


- δ-doping → R_{sd} ↓
- Dry gate recess allows to remove δ-doping
- Impact on the intrinsic fin transport

W_F=5 nm FinFET: Electrical characteristics: δ-doped vs. undoped





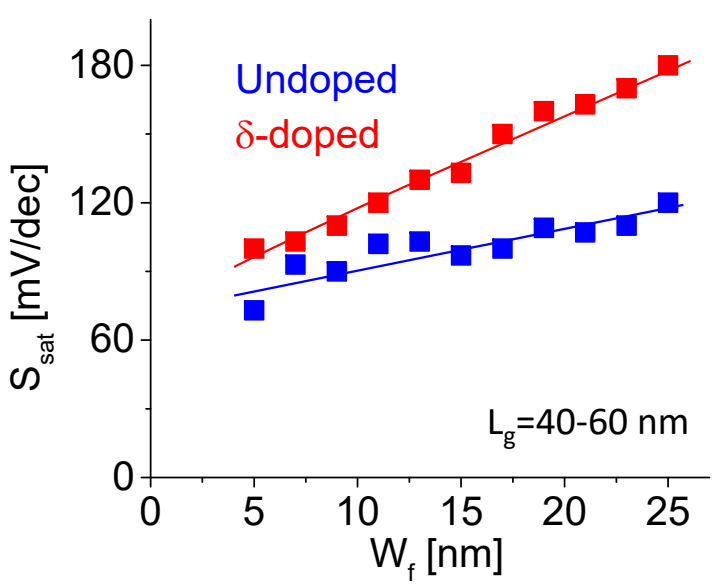


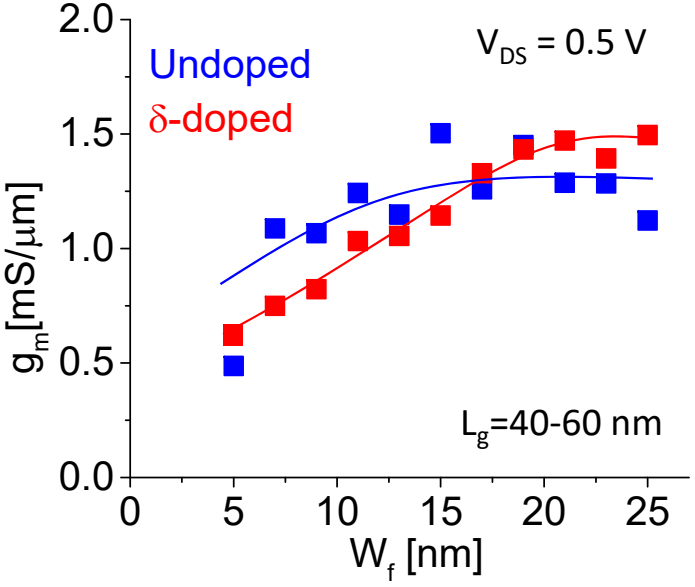
Normalized by gate periphery

Undoped fins:

- better OFF performance
- Undoped Similar ON performance

Electrical characteristics: δ-doped vs. undoped

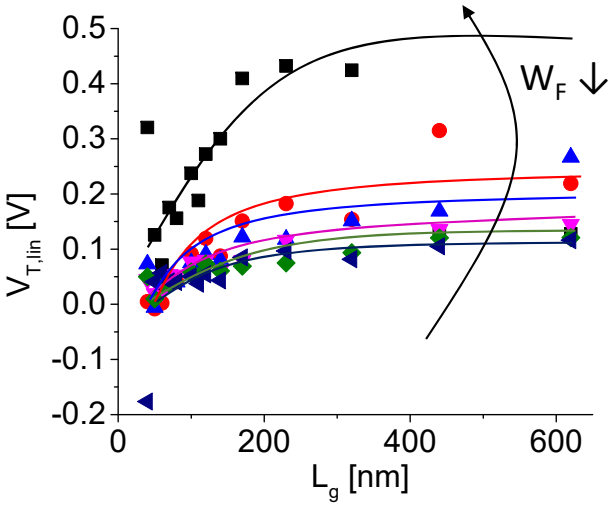




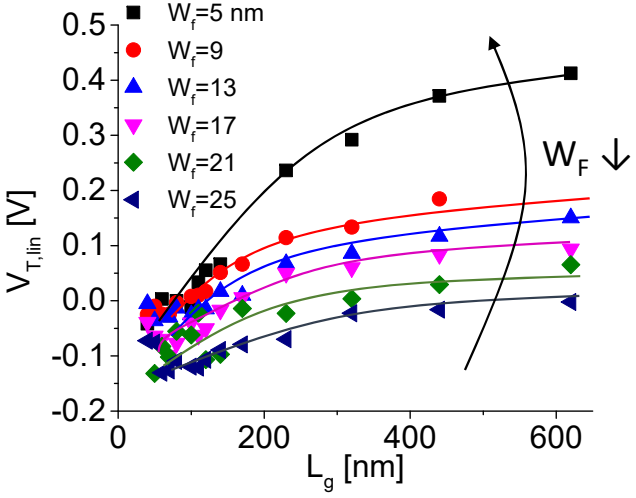
- Undoped fin: improved electrostatics
- For W_f<20 nm undoped-fin ON performance also better

Electrical characteristics: V_T rolloff

Undoped



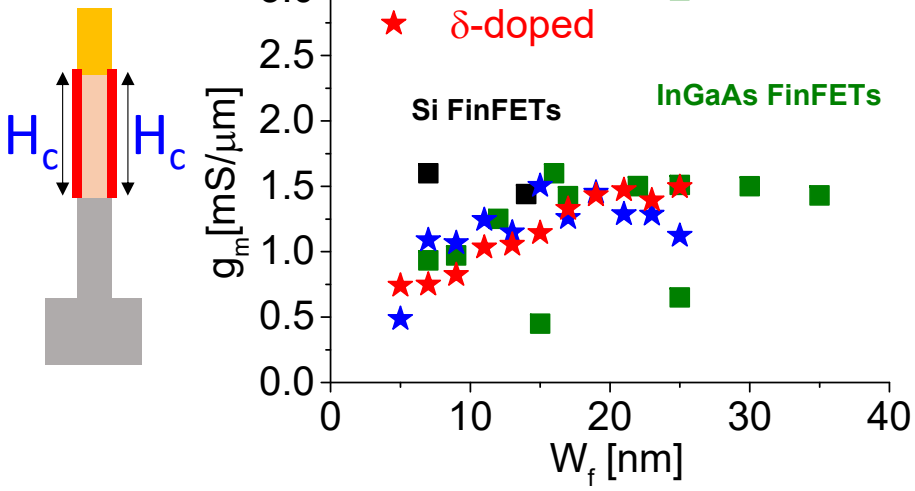
δ-doped



Undoped fins smaller variation of V_T with W_F → Improved V_T rolloff

Benchmarking

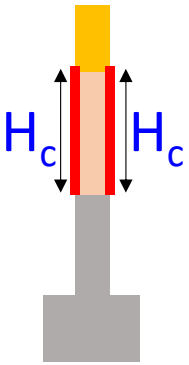
normalized by gate periphery

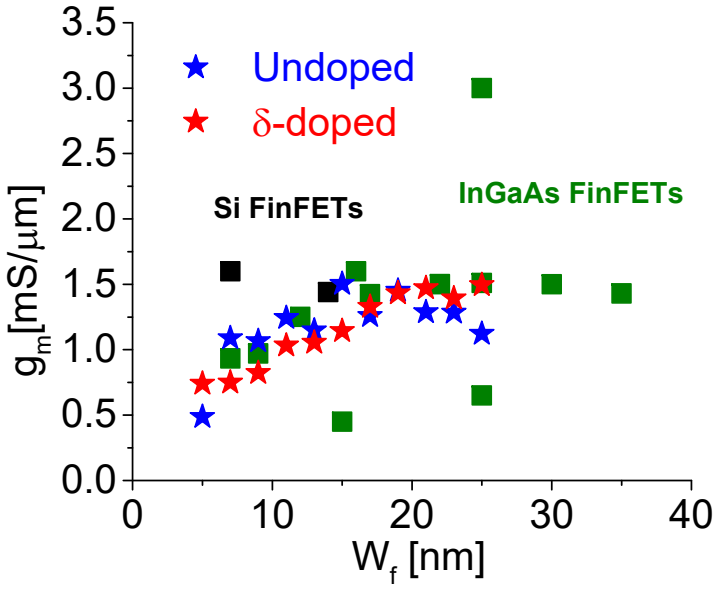


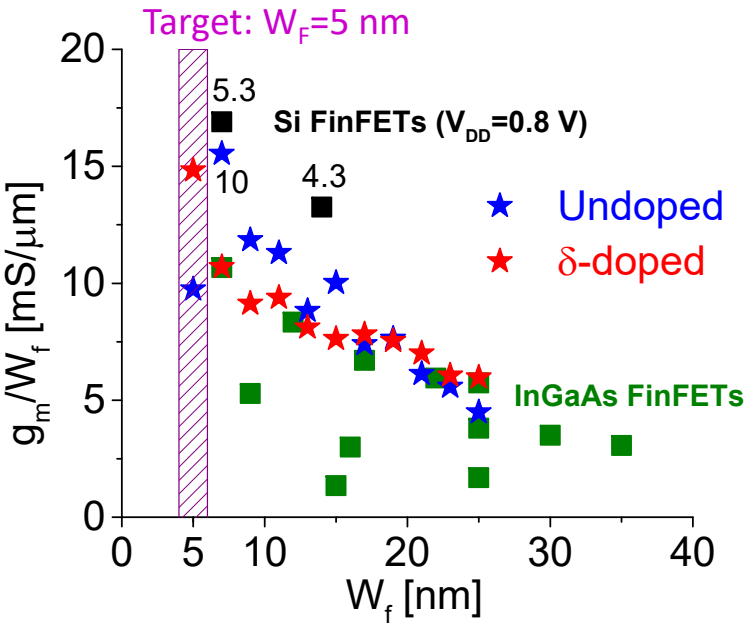
- Systematic g_m degradation for W_f < 15 nm for both δ-doped and undoped structures
- No improvement from increased #DE cycles
- Higher EOT → lower g_m w.r.t. to Gen. 1

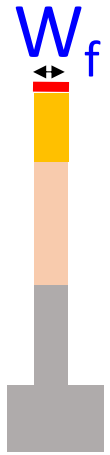
Benchmarking

normalized by gate periphery





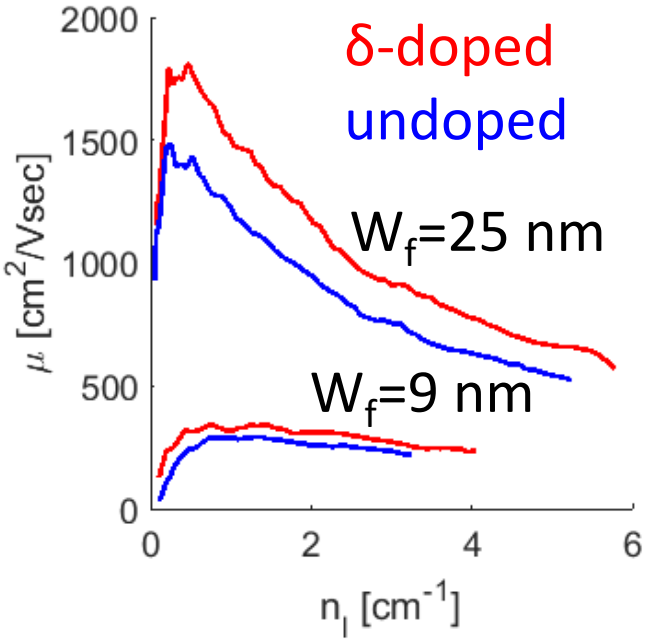




- Record W_f with good electrical performance
- Approaching Si FinFETs even at V_{DD}=0.5 V
- Record AR=10

Long-channel Mobility vs. W_f

Capacitance measured @ 1GHz

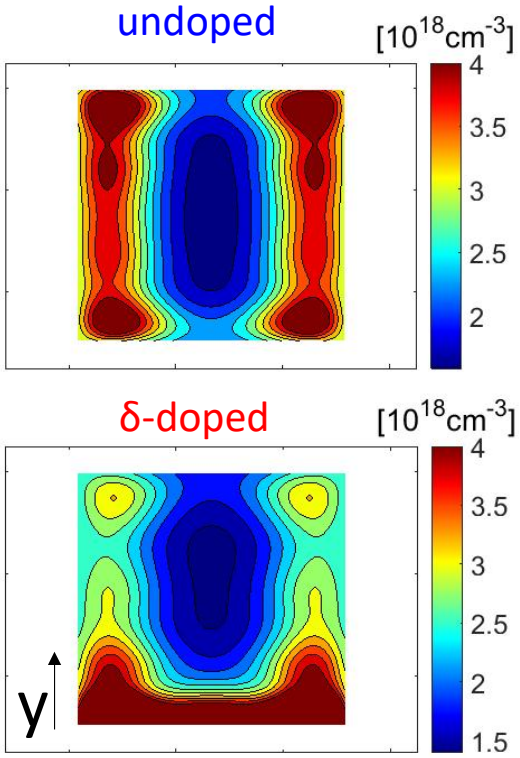


- Strong μ degradation as W_f ↓
- W_f < 10 nm → μ independent of n_l

Simulations – charge distribution

ON state: n_l=3x10^7 cm^{-1}

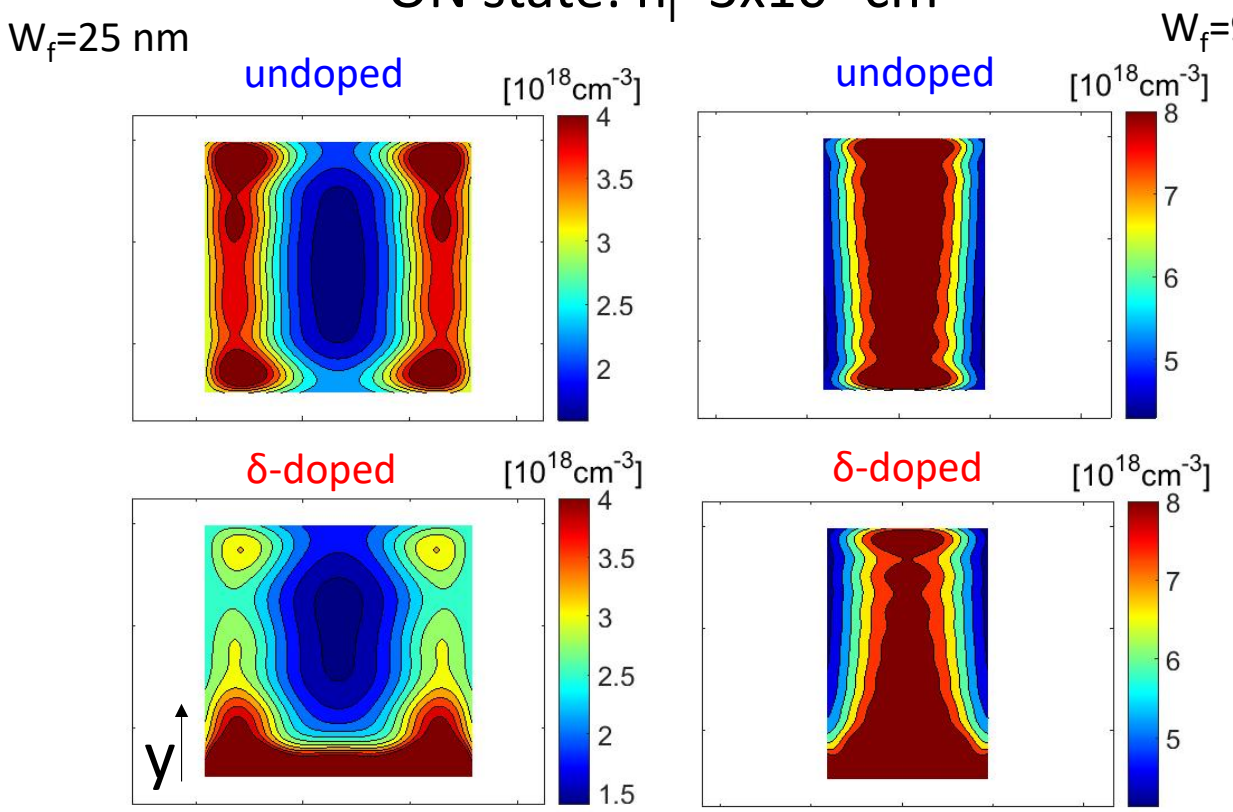
W_f=25 nm



- Undoped fin: better use of sidewalls
- δ-doped fin: conduction close to lower facet of channel

Simulations – charge distribution

ON state: n_l=3x10^7 cm^{-1}

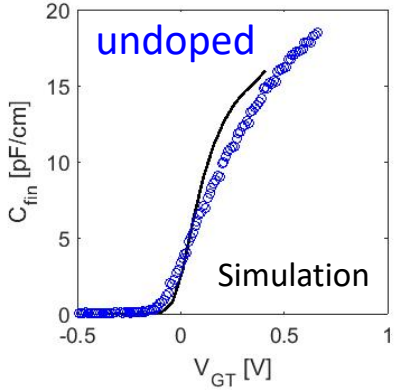


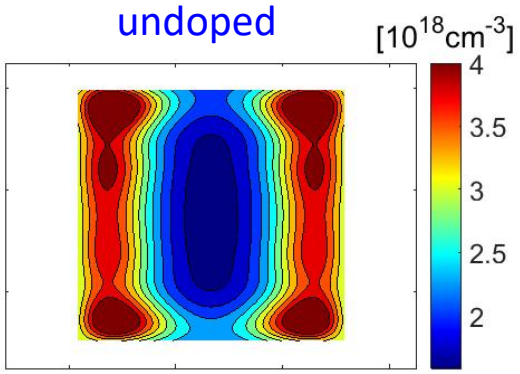
- Narrow fin: volume inversion in both δ-doped and undoped fins

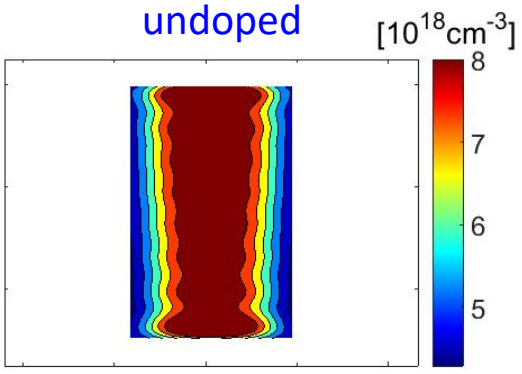
Simulations – capacitance

ON state: n_l=3x10^7 cm^{-1} (V_{GT}~0.4V)

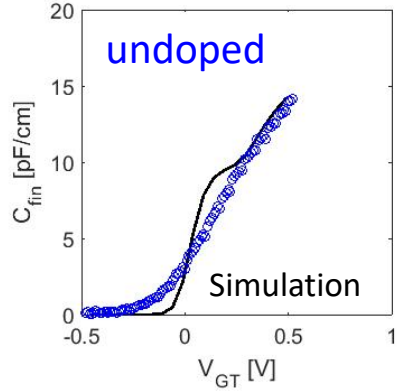
W_f=25 nm

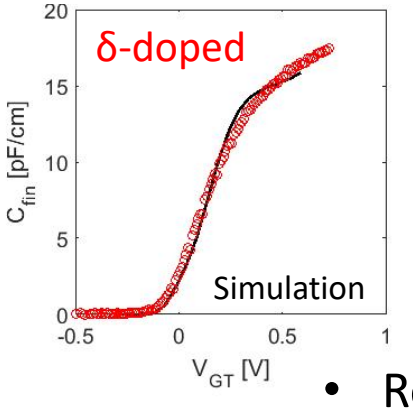


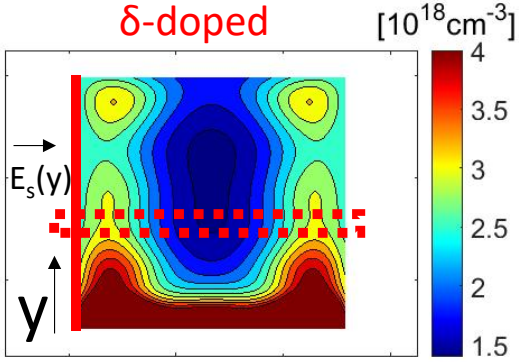


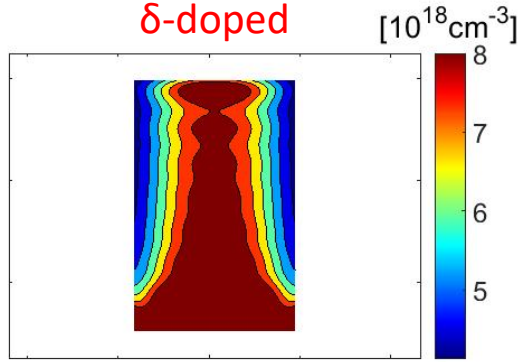


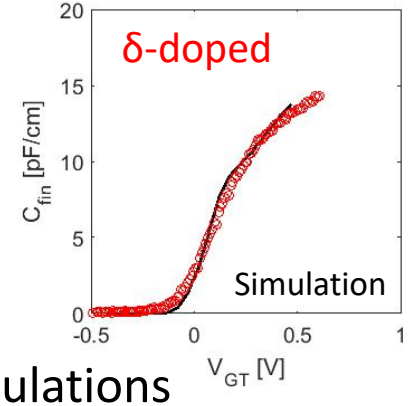
W_f=9 nm





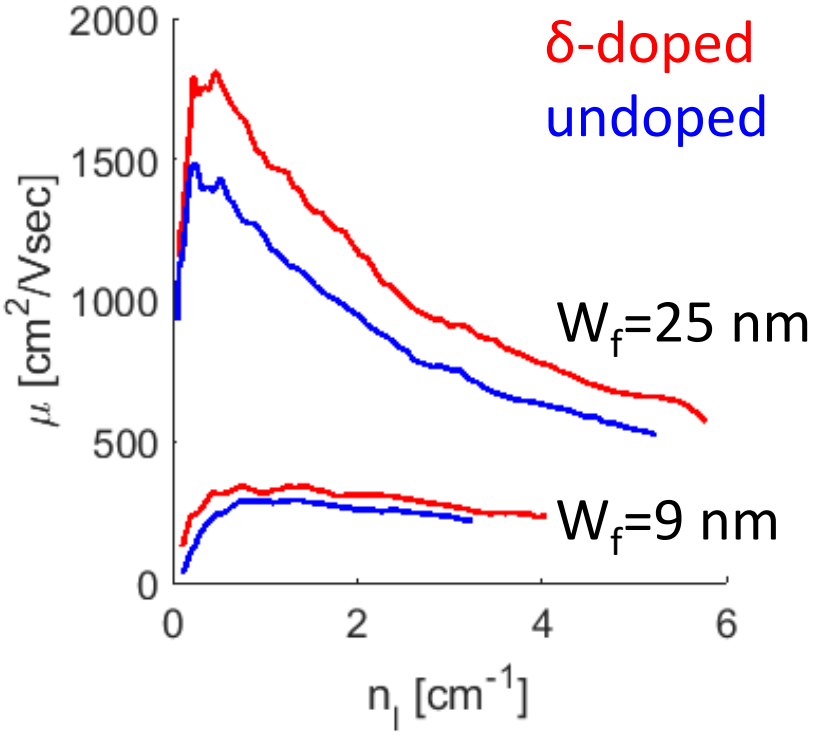


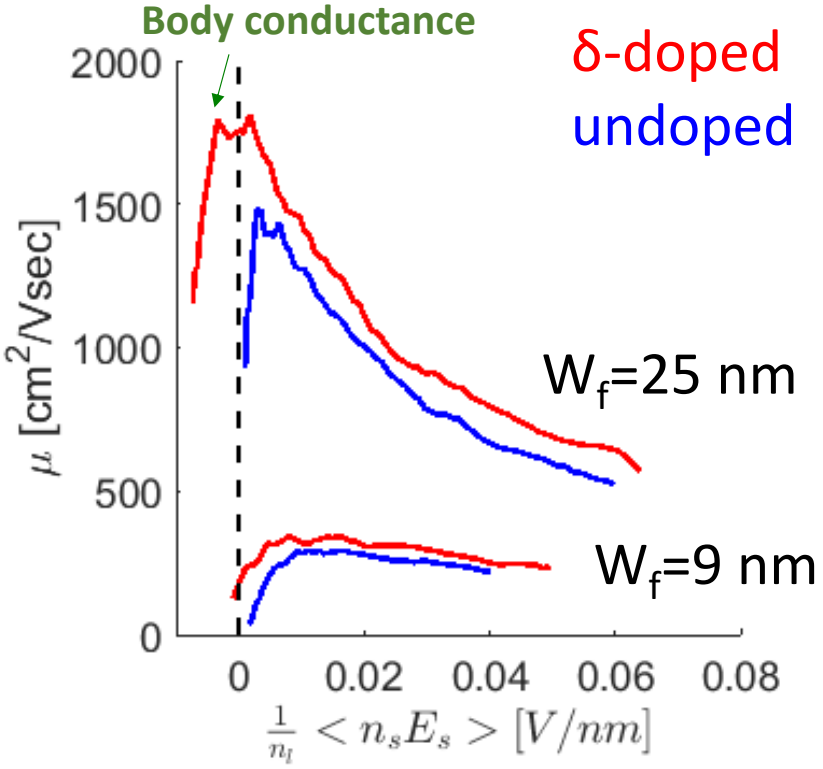




- Reasonable agreement between measurement and simulations
  → extract n_l - E_s relation

Simulations – Mobility vs. Field

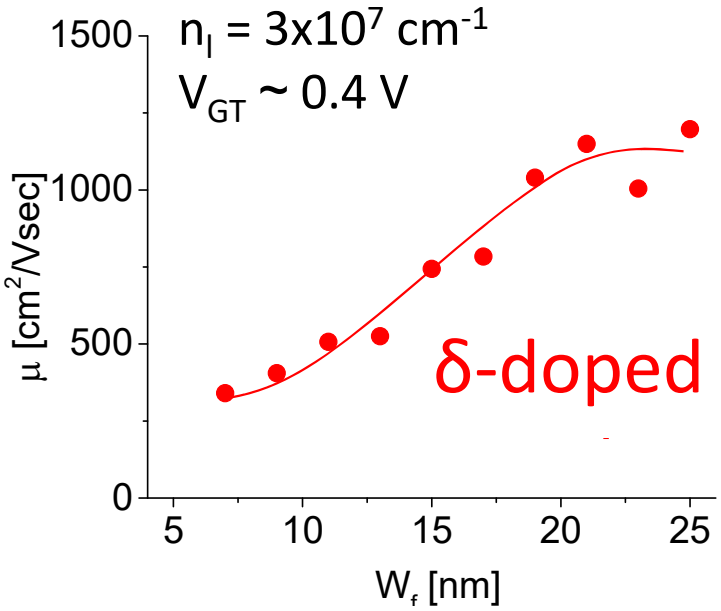


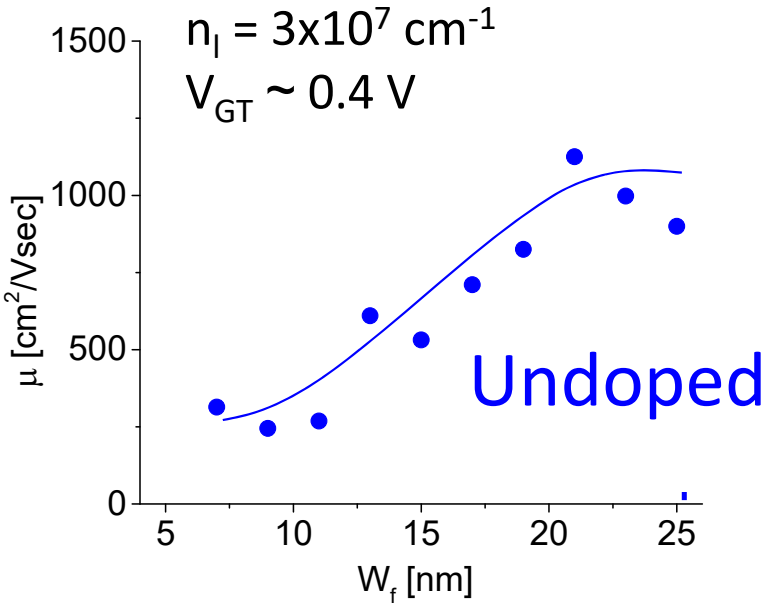


At similar n_l :

- Wide fin: E_S (δ-doped) < E_S (undoped)
- Narrow fin: E_S (δ-doped) ~ E_S (undoped)

Long-channel Mobility vs. W_f





- Large over drive: μ(δ-doped) ~ μ(undoped)
- Strong μ degradation as W_f ↓
- W_f < 10 nm → μ saturate

Conclusions

- Self-aligned gate-last InGaAs FinFET:
  - Self-aligned gate and contact trough precision RIE and digital etch
  - Record AR=10
- Record W_f =5 nm InGaAs FinFET with good electrical performance
- Performance enhancement in narrow fins via δ-doping removal

Thank you !